CLAIMS

1. A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias isolated from each other by an air dielectric; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

2. A semiconductor device as recited in claim 1, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

3. A semiconductor device as recited in claim 1, wherein the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

4. A semiconductor device as recited in claim 1, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

5. A semiconductor device as recited in claim 4, wherein the plurality of supporting stubs further support the passivation layer.

6. A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

7. A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

8. A semiconductor device as recited in claim 6, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

9. A method for making a semiconductor device, comprising:

forming transistor structures on a substrate;

forming interconnect metallization structures in a plurality of levels, the forming of the interconnect metallization structures includes,

depositing a sacrificial layer;

performing a dual damascene process to etch trenches and vias, and

filling and planarizing the trenches and vias,

etching away the sacrificial layer throughout the plurality of levels of the interconnect metallization structures, the etching leaving a voided interconnect metallization structure; and

filling the voided interconnect metallization structure with low K dielectric material, the filling configured to define a low K dielectric interconnect metallization structure.

10. A method for making a semiconductor device as recited in claim 9, further comprising:

forming a passivation layer over the filled voided interconnect metallization structure.

11. A method for making a semiconductor device as recited in claim 9, wherein the sacrificial layer is a dielectric.

12. A method for making a semiconductor device as recited in claim 11, wherein the dielectric is silicon dioxide (SiO2).

13. A method for making a semiconductor device as recited in claim 9, wherein the etching away includes,

subjecting the sacrificial layer to a wet etchant.

14. A method for making a semiconductor device as recited in claim 13, wherein the wet etchant is a mixture of hydrofluoric acid (HF) and de-ionized water (DI water).

15. A method for making a semiconductor device, comprising:

forming transistor structures on a substrate;

forming interconnect metallization structures in a plurality of levels, the forming of the interconnect metallization structures includes,

depositing a sacrificial layer;

performing a dual damascene process to etch trenches, vias, and stubs, and

filling and planarizing the trenches, vias, and stubs,

etching away the sacrificial layer throughout the plurality of levels of the interconnect metallization structures, the etching leaving a voided interconnect metallization structure and supporting stubs.

16. A method for making a semiconductor device as recited in claim 15, further comprising:

forming a passivation layer over the voided interconnect metallization structure and supporting stubs.

17. A method for making a semiconductor device as recited in claim 16, wherein the voided interconnect metallization structure has one of air, nitrogen, neon, and argon as a dielectric.

18. A method for making a semiconductor device as recited in claim 15, wherein the etching away includes,

subjecting the sacrificial layer to a wet etchant.

19. A method for making a semiconductor device as recited in claim 18, wherein the wet etchant is at least a mixture of hydrofluoric acid (HF) and de-ionized water (DI water).

20. A method for making a semiconductor device as recited in claim 15, wherein each of the supporting stubs is configured to form a supporting column that extends through the plurality of levels of the voided interconnect metallization structure.